DesignCon 2009

Noise Injection for Design Analysis and Debugging

Douglas C. Smith, D. C. Smith Consultants
[Email: doug@dsmith.org, Tel: 408-356-4186]

Abstract

Troubleshooting PCB and system designs, especially for intermittent errors, can be time consuming and predicting potential field problems even more difficult. A method is presented that is useful in finding both system design problems and layout defects in PCB designs as well as gauge the risk of potential field problems. The method involves inductively injecting controlled voltage pulses into individual paths on a PCB or into a system component using a specific methodology, a square wire loop, and high voltage pulse generator with an output having a risetime of a few nanoseconds and a fall time of several tens of nanoseconds. This method has been very successful in finding design problems in PCBs.

Author(s) Biography

Mr. Smith has worked over four decades specializing in high frequency measurements, circuit/system design and verification, switching power supply noise, EMC/ESD, and immunity to transient noise. He has lectured at many universities and delivered public and private seminars. He maintains a popular website devoted to high frequency measurements and troubleshooting, http://www.dsmith.org.

Background and Tools

The method presented in this paper has been able to find design problems on PCBs and in systems that defied traditional troubleshooting methods. Before jumping into the method and examples, I will cover some background.

The main tool that will be used in this troubleshooting method is a square magnetic loop, a fancy name for a square wire loop, connected to a suitable pulse generator. So first, let's look at this tool and how it works as well as some simple theory of operation.

The Square Wire Loop

Figure 1 shows an example of a square wire loop about 2.5 cm on a side. It is made by starting with a straight piece of 16 AWG stiff brass wire soldered to a BNC barrel adapter. The finish on the BNC adapter should be roughed up with sand paper before soldering to insure a secure solder joint. Then, heat shrink tubing is placed on the wire and finally, the wire and tubing are bent around in a square shape and plugged into the center pin opening of the BNC adapter. 16AWG wire is used because it just fits in the BNC center pin opening. It is not necessary for the loop to be symmetrical with the BNC connector as shown in Figure 1. So, after soldering, the first and second bends (bare wire) are not needed, just take the wire straight up from the solder joint and form a flag shaped loop. This saves a little time and allows the heat shrink tubing to completely cover the loop without having to make two 90-degree bends close to each other.

Figure 1, Example of a square wire loop

Figure 2 shows an end-on view of a smaller loop, about one cm on a side. In this view, one can see the brass wire just fitting the center conductor opening of the BNC connector. Sometimes smaller loops like this one are needed to get into tight spots on a PCB.

Figure 2, Example of a smaller loop – end-on view

Inductive and Capacitive Coupling

To understand how the method is applied to a circuit board, it is necessary to understand how inductive and capacitive coupling work. Let's start with capacitive coupling as illustrated in Figure 3.[1]

In this example, a signal is capacitively coupled into a circuit with load impedances on the right and left. The injected signal is a current and if the circuit is symmetrical, the two Z_Ls are the same, then the current flowing to the left will equal in magnitude the current flowing to the right. Note that the injected currents are flowing in opposite directions. Contrast this situation with that of inductive coupling shown in Figure 4.
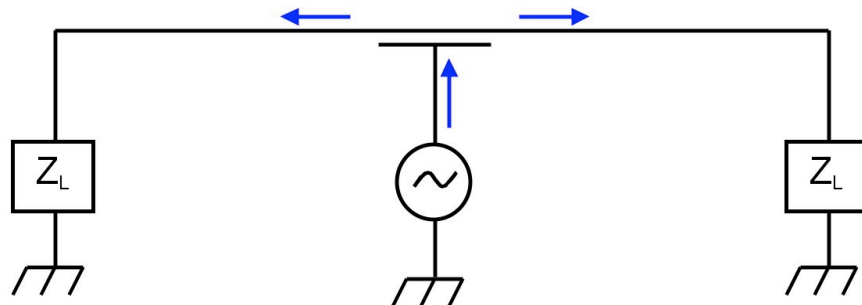

Figure 3, Capacitive coupling

In Figure 4, the signal is coupled inductively into the loads using a transformer. The signal source is coupled into the loads as a voltage in series with the two loads. Whether the two loads are the same impedance (symmetric circuit) or not, the two currents to the left and right of the coupling point will be the same amplitude. Note that for inductive coupling, the current directions are the same.
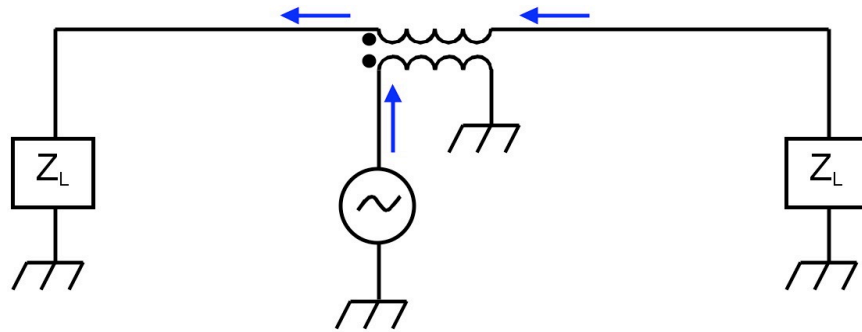
Figure 4, Inductive coupling

Sometimes structures that do not look like transformers actually are. The wire loops in Figures 1 and 2 are cases in point. Figure 5 shows the result of positioning a loop next to a conductor. If the di/dt of the signal generator output is high enough, a substantial Ldi/dt voltage drop can be developed across each leg of the square loop. The side of the loop closest to and parallel to the conductor connecting the two loads will induce a fraction of its Ldi/dt drop into the conductor as Mdi/dt. Induction from the other three sides is small for a square loop, the most being from the opposite side of the loop.

For a positive pulse, the voltage drop across the face of the loop closest to the conductor will be as shown in Figure 5, + to – from left to right as will be the induced voltage in the conductor. But, the voltage across the face of the loop is a voltage drop and the voltage in the conductor connecting the loads is a source, so the current in the conductor flows from right to left, the opposite direction of the current in the loop.
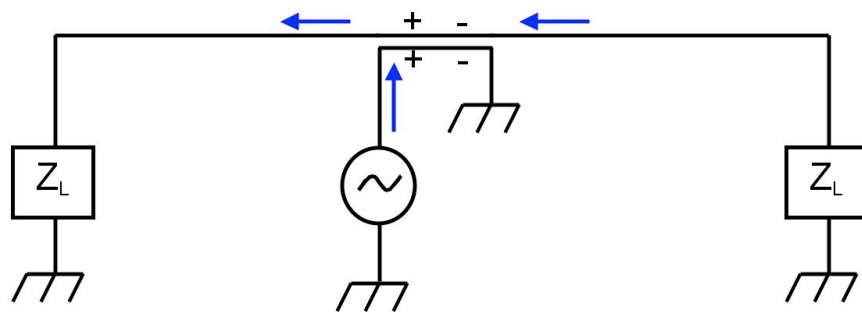

Figure 5, Example of induction from a square wire loop

The Ideal Pulse Source

To develop the ideal pulse shape for the troubleshooting method, consider the test setup in Figure 6. The pulse source can be either an Electrical Fast Transient (EFT) Burst, IEC 61000-4-4, generator or a Fischer TG-EFT generator, shown in Figure 6. The IEC 61000-4-4 test is one of the immunity standards required for CE compliance of a product [2,3]. The generator can be found in most EMC compliance labs.

What makes these generators ideal for this use? The main parameters are the pulse shape of the generator output and its high amplitude. In Figure 6, a square wire loop is connected to a TG-EFT pulse generator with a current probe clamped around the wire loop and connected to the 50 Ω input of an oscilloscope to measure the current flowing in the loop. A close-up of the loop and current probe is shown in Figure 7.
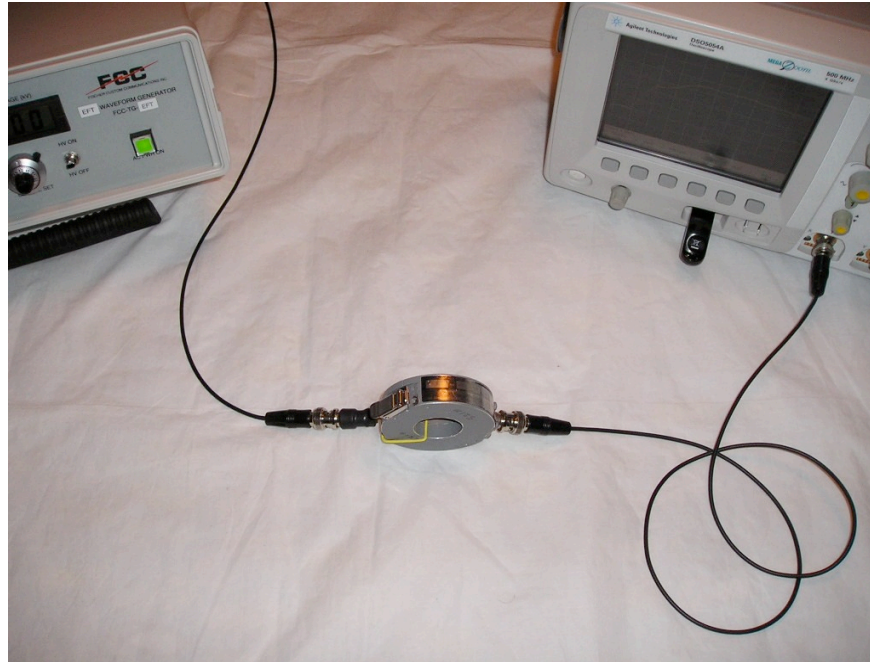

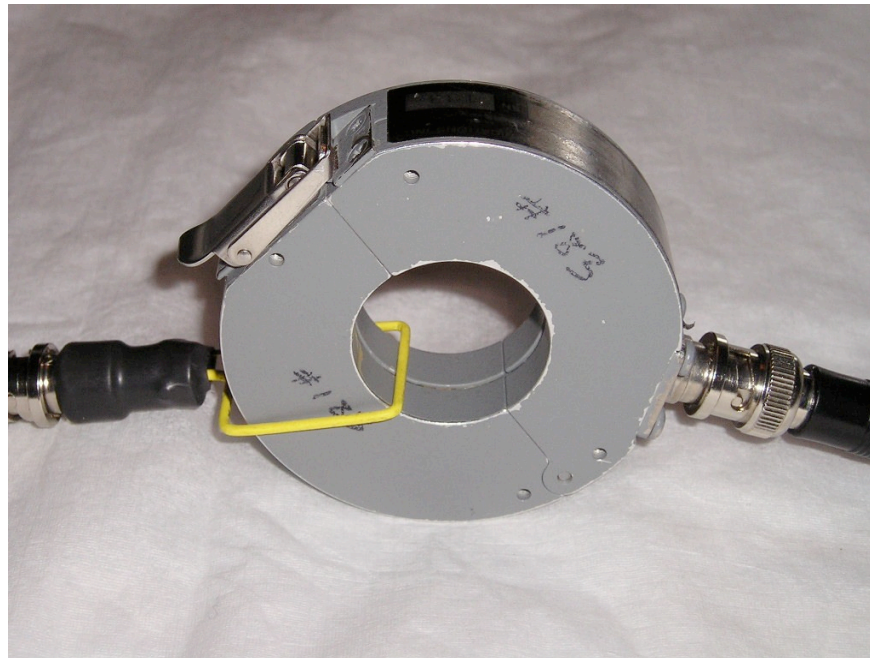Figure 6, Test setup to measure pulse characteristics

Figure 7, Close-up of loop and current probe

Figure 8 shows the resulting current. Notice the current has a fast risetime and a much slower fall time. The dip to negative current is an artifact of the AC coupled nature of the current probe causing the area above ground in the plot having to be equal to the area below ground in the plot. Why this shape is important can be seen in Figure 9.
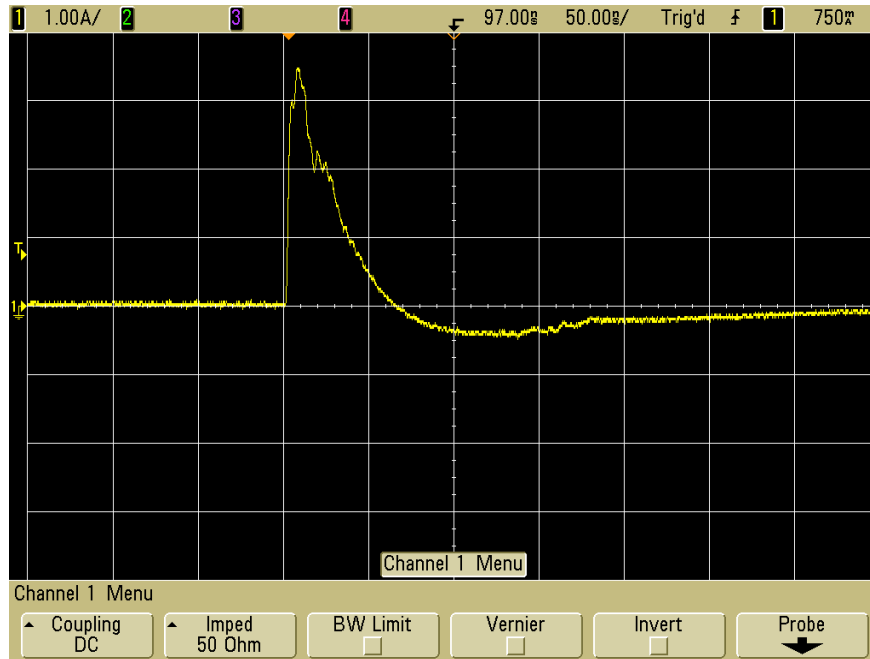

Figure 8, Measured current in loop for generator setting of 100 Volts peak
(Vertical scale = 1 Amp/div, Horizontal scale = 50 ns/div)

In Figure 9, the current waveform is spread out to 10 ns/div and the time derivative of the current is calculated in the oscilloscope and shown as well. The current waveform shows a few nanosecond rise to about 3 Amps and the derivative, di/dt, is mostly just a single positive pulse with some lower amplitude noise corresponding to features along the top current waveform. Since the loop injects a voltage of Mdi/dt into a nearby circuit, the injected pulse will look the same as the di/dt plot in Figure 9. The shape of the induced voltage pulse is important. The injected voltage is a unipolar pulse whose polarity can be reversed by simply rotating the loop 180 degrees.

One should be able to easily measure this result directly. A way to do this is shown in Figure 10. Two square loops are held adjacent with one connected to an EFT pulse generator and the other to the 50Ω input of an oscilloscope (both using good quality 50Ω coax cable). The result can be seen in Figure 11 showing a peak voltage of about 4 Volts for a 250 Volt open circuit EFT generator setting.

Figure 11 looks very much like the di/dt pulse in Figure 9, although reversed in polarity because of the relative loop orientations. The single polarity induced voltage pulse is important to the troubleshooting method to be described.
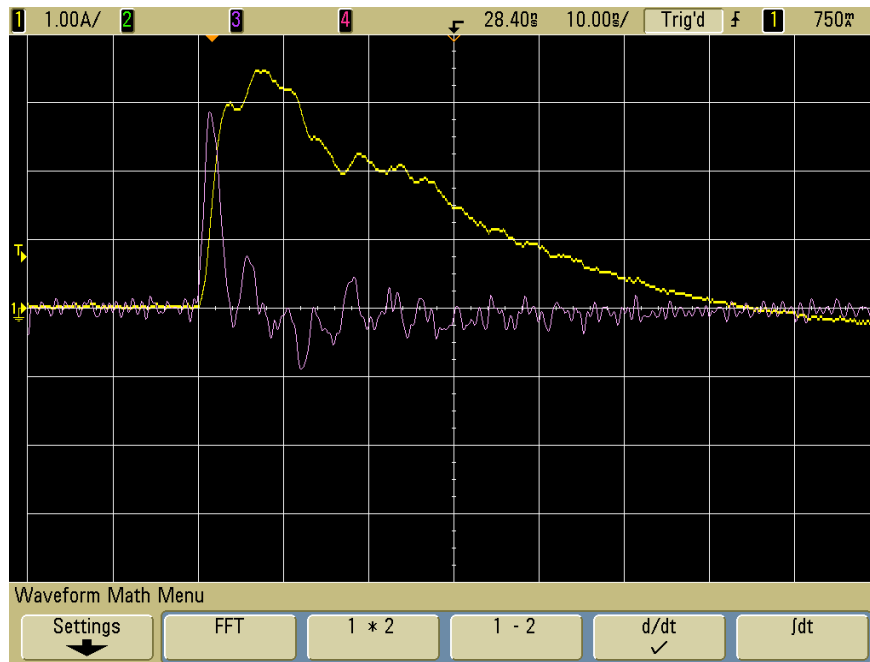
Figure 9, Measured current in loop for a TG-EFT generator setting of 100 Volts peak showing the time derivative of the current as well
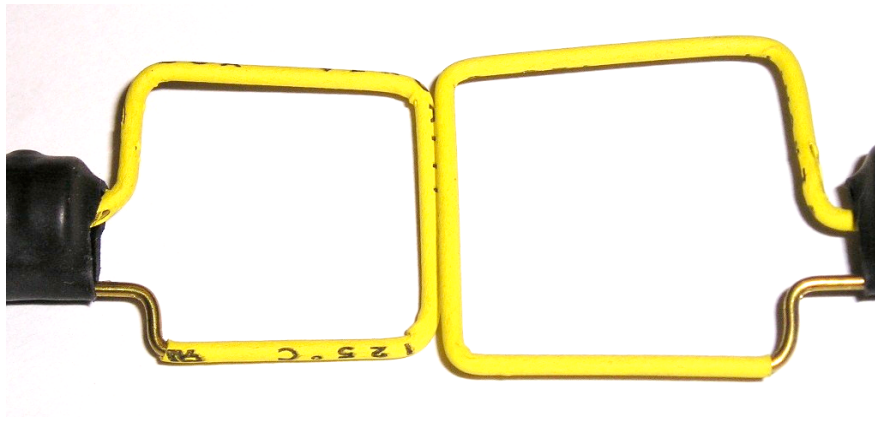(Vertical scale = 1 Amp/div, Horizontal scale = 10 ns/div)

Figure 10, Measuring loop induction into a second loop

An important advantage of injecting pulses inductively this way into circuits is that the original circuit conditions are not affected since no connection to the circuit is made. In addition, mutual inductance falls off quickly with distance, so the pulse injection is very specific to the conductor adjacent to the loop. Since the TG-EFT has a risetime (~2 ns) about twice as fast as an EFT generator (~5 ns), the di/dt of the TG-EFT is about twice the value for the same voltage setting. The range of settings I use for finding problems with a 2.5 cm loop is 100-500 Volts for the TG-EFT and 250-1000 Volts for an EFT generator. **Caution: since these generators have a high open circuit voltage, it is important that the grounded side of the loop be securely soldered to the BNC or other connector.**
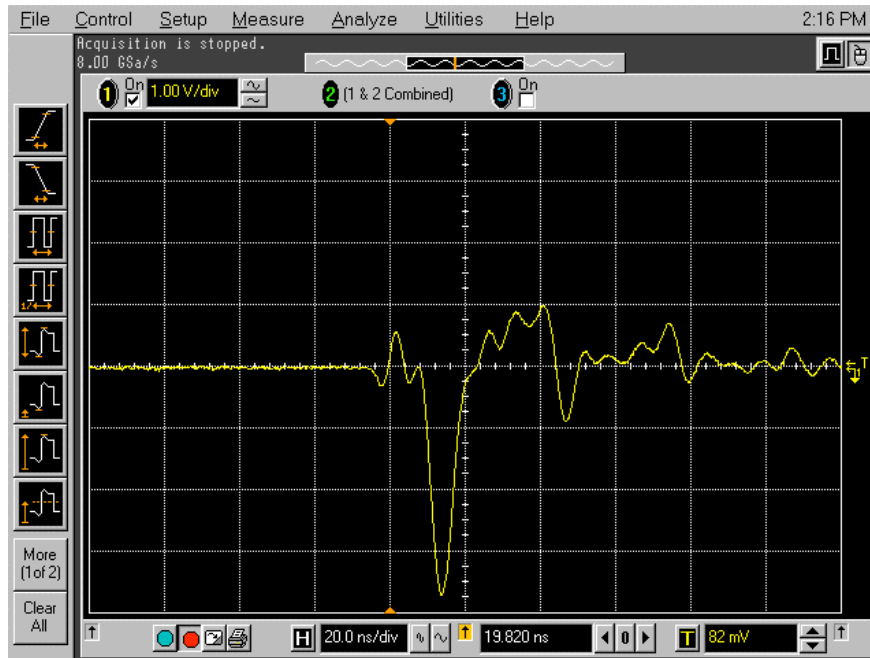
Figure 11, Induced voltage in second loop using an EFT generator to feed the first loop.

Troubleshooting Method

The method to be described below is applicable to both PCBs and other system components. Let's look at PCBs first.

Application to a PCB

The application of the method to a PCB is as follows.

1. Using two loops, as in Figure 10, set the pulse generator to give an induced voltage of around 4 Volts peak. This will require a setting of the TG-EFT generator of around 100 Volts and a setting of about 250 Volts on an EFT generator.
2. With the board operating, scan the board with the square loop, then rotate the loop 90 degrees and repeat to get both X and Y paths on the board. See Figure 12.
3. Rotate the loop 180 degrees and repeat #2 to inject the opposite polarity pulses.
4. Gradually increase the generator setting and repeat steps #2 and #3. The amount of increase will depend on how much resolution is desired. Normally I use 100 to 200 Volts for the TG-EFT and about double that for the EFT generator. The higher voltage settings for the EFT generator are needed because the risetime is somewhat slower on the EFT generator and require higher settings to achieve the same di/dt values as described earlier.
5. Note both the operational symptom and generator setting when an effect on the PCB is first noted.

If a TG-EFT generator is used, set the pulse repetition rate to several pulses per second so that as the loop is slowly moved, each part of the circuit is exposed to the stress. If an

EFT generator is used, the default burst rate of 5 kHz for 15 ms repeated three times per second is good without modification.
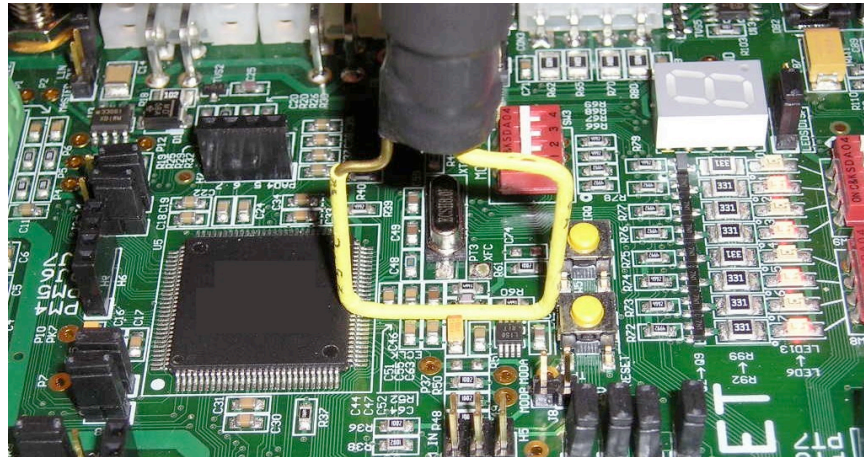

Figure 12, Applying induced voltage pulses to a PCB

Application to an IC Package

The application of the method to an IC package is also possible and is illustrated in Figure 13. In this case, the loop is sized to the IC package and rotated around while applying pulses. One could make a loop one half the package size and rotate the loop around the package while holding one corner at the center of the package. This will give better resolution on which part of the package is most sensitive.

This method works best for flat packs and works for ball grid arrays, but access to the top of the package is required. If a heat sink or metal heat spreader is used, it will need to be removed to perform the test, as the metal will short out the fields generated by the loop.
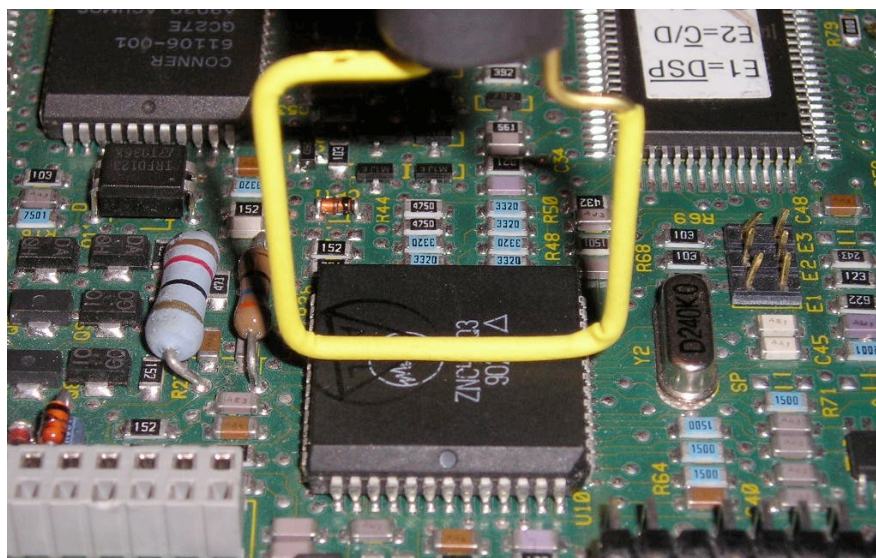

Figure 13, Applying induced voltage pulses to an IC package

Application to a Flat Cable

The application of the method to flat cable is also possible and is illustrated in Figure 14. This test is very sensitive and can find problematic signals quickly. One should have no trouble resolving a problem to a single conductor in the cable if the generator output is set to the minimum required for a response from the circuit.
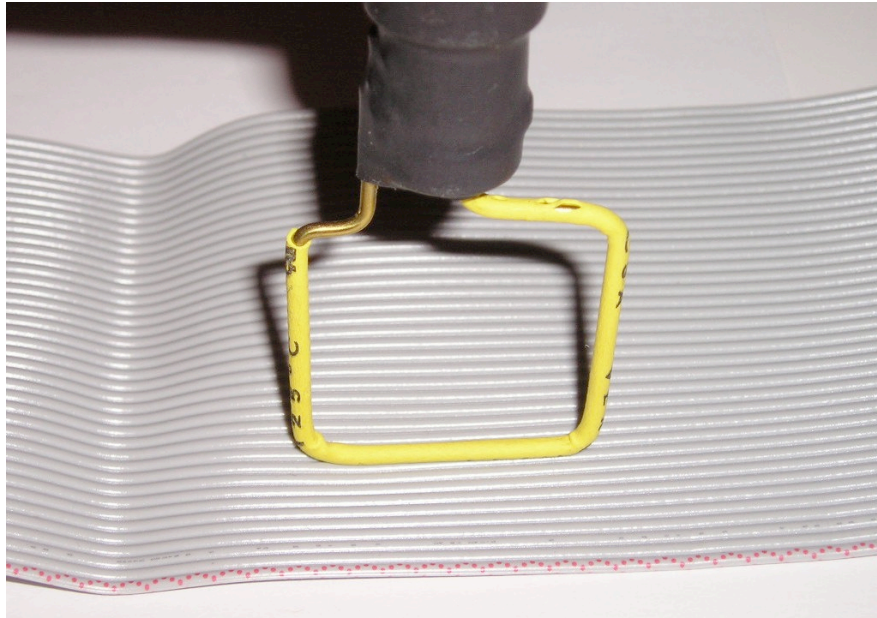

Figure 14, Applying induced voltage pulses to a flat cable

For both the flat cable and IC device package, the general method is similar to that for PCBs. That is to start with a low generator setting and gradually work up in amplitude until a response is observed. For an existing problem, if the first symptom is the same as the problem, the portion of the circuit involved with the problem is likely that receiving the pulse injection from the loop. When checking for potential problems, the amplitude that causes circuit affects to appear gives a relative risk of field problems. This is discussed in Case 1 below.

Results

The methods described have been very successful at finding design problems in equipment. Both compliance test problems and field problems have been solved. A few cases are in order.

Case 1: A system design utilized two PCBs, one containing the processor and associated circuitry and the other containing noisy relays to control high powered circuits in the system. The system was experiencing strange states that caused disruption of the intended function due to ESD events that occurred naturally as a result of everyday operation of the equipment. In the process of scanning the flat cable connecting the two PCBs, it was noted that the tenth line from one side was very sensitive to induction from the loop, which caused resets and other strange operation. Upon consulting the wiring diagram, it

was determined that the tenth line was the processor reset lead! It is not good design practice to run the processor reset lead off the board to another board full of noisy relays!

One could certainly find a problem like this with enough time spent pouring over system wiring diagrams, board layout plots, and schematics. However, this particular problem was found in a couple of minutes after starting to scan with the loop, much faster than looking at wiring diagrams first, hoping to spot the problem.

The level of drive used to cause the problem to occur was a setting of about 170 Volts (open circuit) from a TG-EFT generator. This would be about equivalent to a setting of 300 Volts from an EFT generator. This is a very low value that I have found to be correlated to system problems in the field. By contrast, I have found that a system that can withstand a drive of 500 Volts from the TG-EFT generator, or 1000 Volts from an EFT generator, applied with a 2.5 cm loop of 16 AWG wire covered with thin heat shrink tubing and applied over all PCBs and other accessible areas (such as flat cables) is generally not going to be a problem in the field.

Case 2: A piece of network gear was occasionally resetting its Power Over Ethernet, POE) circuits at random times in the field in a number of installations. The system survived EFT testing to the maximum level of the generator, 4400 Volts, over four times the requirement for CE marking of that system. The EFT test was done to this high level to rule out impulses on the power mains or Ethernet cables that might be causing the problems.

In less than an hour's work, scanning with a 2.5 cm square loop fed with about 500 Volts from the EFT generator, a sensitive area of the circuit board was found. It was also noted that there was a position for a bypass capacitor that was not populated in the same area. Installation of the capacitor eliminated the sensitivity to the loop injection and solved the field problem as well. The injection test plus adding the capacitor and retesting took less than a morning's work and yet solved a problem that seemed intractable in the field.

These two cases are representative of many that have been solved using this method, including many cases of layout problems on PCBs that were generally well designed except for a single weak spot. Paths crossing cuts through the power and ground planes are very easily spotted using this method. Being able to inject pulses of known polarity is also useful as it can help understand the mechanism of the problem. For instance, pushing a normally high logic signal higher is not as much of a problem as pulling a high signal to a low state.

Summary and Conclusions

The method of inducing pulses of known polarity and amplitude into circuits described has been shown to be very useful in finding system problems and predicting problems that have yet to surface. One of the main features of this way of injecting pulses is that the original circuit conditions are not affected to a significant extent since no contact is made to the circuit.

This method can be applied at the system, PCB, and IC package level making the method very flexible and useful. Many system problems have been solved in less than a day's work that had not yielded to, in the worst cases, months of work using conventional troubleshooting methods.

References

[1]   "Inductive and Capacitive Coupling – Induced Current Characteristics," April 2005 Technical Tidbit article, http://emcesd.com/tt2005/tt040205.htm

[2]   A brief description of the IEC 61000-4-4 test can be found at: http://www.thermo.com/com/cda/products/product_application_details/1,1063,11367,00.html

[3]   Fischer Custom Communications, http://www.fischercc.com, Torrance, CA.

[4]   Figures used are from Technical Tidbit articles at http://emcesd.com and seminar notes by Douglas C. Smith, used with permission.