ESD Immunity in System Designs, System Field Experiences and Effects of PWB Layout

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Abstract **-** Soft errors as well as damage can be caused by ESD in electronic systems. Such effects have resulted in many problems with companies and customers incurring large costs. Effects on system immunity from printed wiring board layout will be covered and examples of field problems described. Suggestions on how to avoid such problems are given.

Introduction

The influence of design at the circuit board and system level on ESD immunity of electronic systems is well documented. However, designers are often forced by cost, time to market, and space limitations to make compromises. Hard data and real experiences on the impact of ESD immunity of circuit board and system design make it easier for designers to make a case to include needed design features.

Data is presented below on two test boards that graphically illustrate how strongly board layout can affect ESD immunity. [1] In addition, experiences in the field are given which reinforce the importance of good design.

Diving Path Test Board

Figure 1 shows a test board that is double sided copper with two test paths. The paths are about 30 cm in length. One path is routed from an SMA connector to a 47Ω load and the other crosses through the two ground planes and travels one third of the distance on the opposite side of the board before reaching the load resistor. The two ground planes are connected together at the SMA connectors and at the load resistors. Small gauge copper wire held in place by tape forms the paths which have a nearly 50Ω characteristic impedance.

ESD current from a 3 kV contact discharge is injected onto the ground plane as shown in Figure 1 at the right edge of the board and exits from the left side.

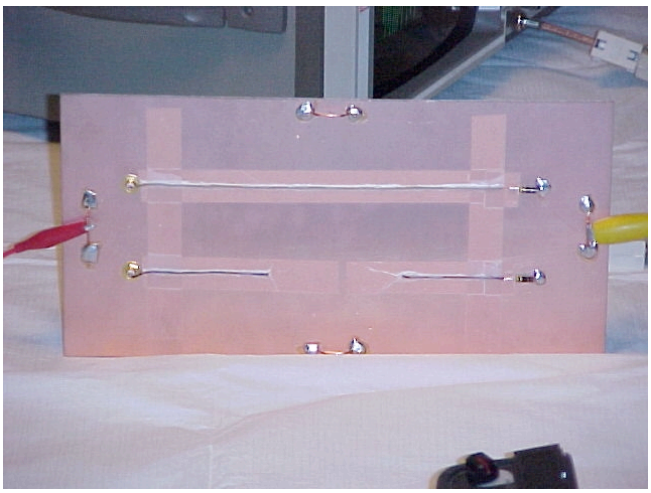

Figure 1. Test Board with Two Test Paths

Figure 2 shows the back of the board and the connection to the scope. Ferrite cores are used to prevent ESD current from diverting to the coaxial cable and the scope chassis. Figure 3 shows the complete test setup.

Figures 4 and 5, respectively, show the apparent signal generated by the ESD across the 47Ω loads for the straight path and the path that crosses through the ground planes. The difference between the two cases is striking.

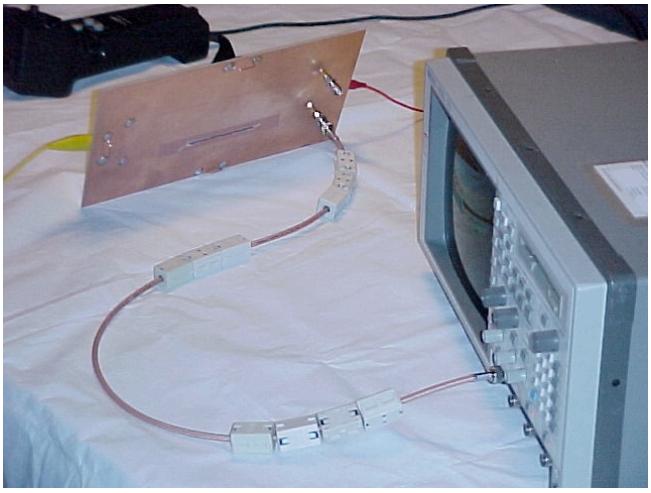

Figure 2. Connection to Oscilloscope

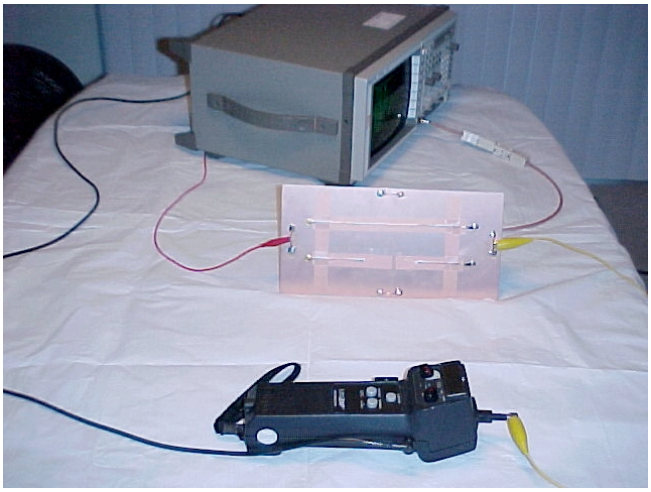

Figure 3. Complete Test Setup

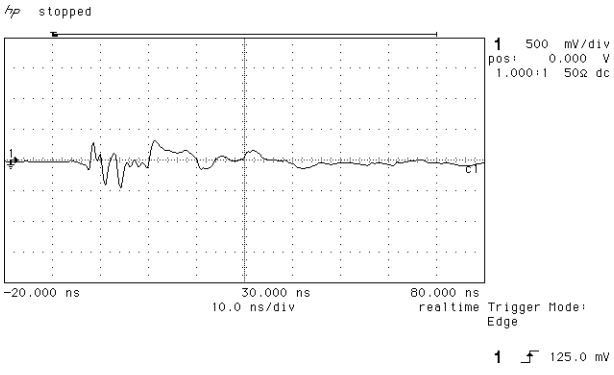

Figure 4. Apparent Signal on Straight Path

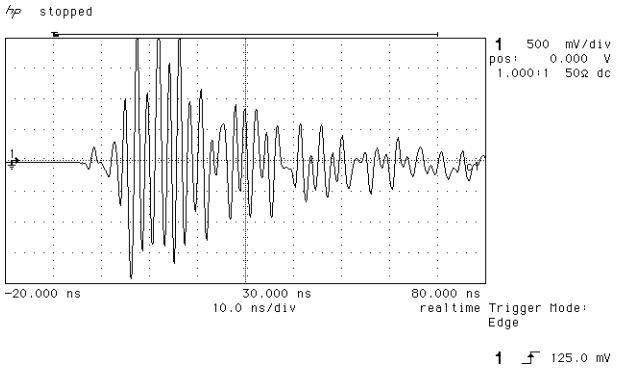

Figure 5. Apparent Signal on Path Crossing Planes

The interference generated in the straight path, Figure 4, was less than 500 millivolts. In the path crossing through the ground planes, the interference was greater than 2 Volts! That value is easily enough to corrupt a 5 volt logic signal.

Crossing through two ground planes (or any conducting planes) puts the interplane impedance in the return path of the signal loop formed by the signal path and its return in the ground plane. As can be seen, this can be a significant effect.

Split Plane Test Board

Figure 6 shows the board use for the test. Construction was similar to the previous test except than one of the paths crossed a break in the ground plane. The board was about 20 cm in length.

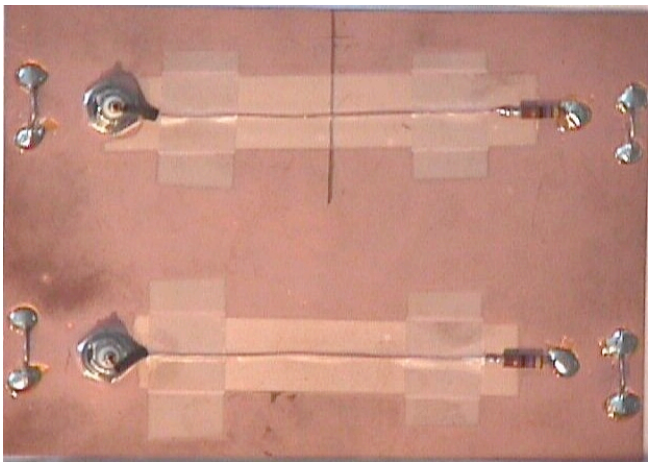

Figure 6. Split Plane Test Board

The test setup is also similar to the first test and is shown in Figure 7. The ferrites used to prevent the ESD current from ending up on the front of the scope are plainly visible.

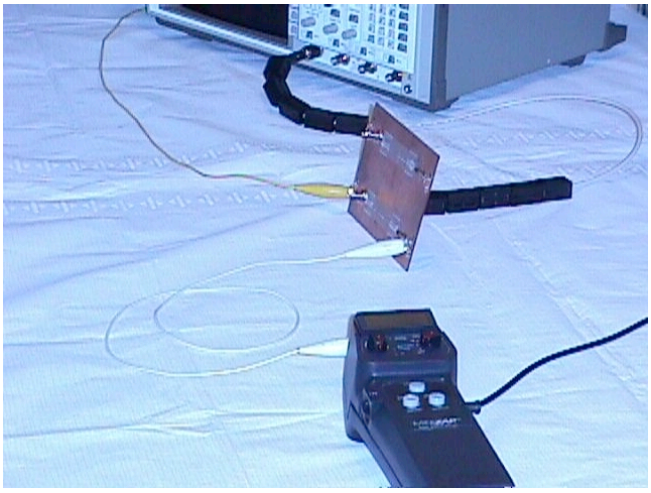

Figure 7. Complete Test Setup for Split Plane Board

Figure 8 shows the interference into the straight path from a 4 kV contact discharge. The amplitude is about 300 mV peak, not enough to be a problem for most logic families.

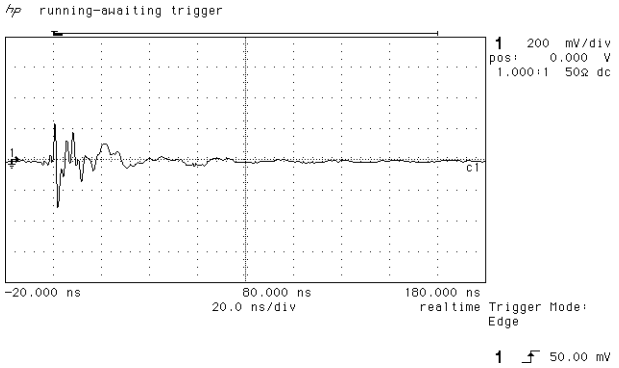

Figure 8. Apparent Signal on Straight Path

Figure 9 shows the interference to the path crossing the break. The amplitude has increased to about 3.5 volts, enough to corrupt most any logic signal!

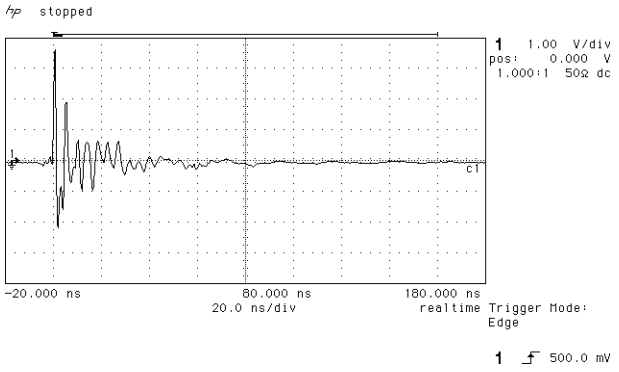

Figure 9. Apparent Signal on Path Crossing Planes

The reason for the large increase is that the signal and it's return path form a large loop. The ESD current must share part of the loop with the signal return. The common part of the loop is on the ground plane around the end of the slit.

Design Examples

Figure 10 shows a circuit board with split ground and power planes. A light is shining on the opposite side of the board and shows where the break in the planes is located. Many paths can be seen crossing the break.

Layout features such as this are a potential source of ESD immunity problems as well as signal integrity and general EMC (electromagnetic compatibility) problems.

Figure 11 shows another example on an older board design. Notice the many leads crossing the break in the ground/power planes. In both design examples one of the paths wanders over a break and then back again when it was not necessary to do this. Design features like this are all too common and can lead to a host of problems.

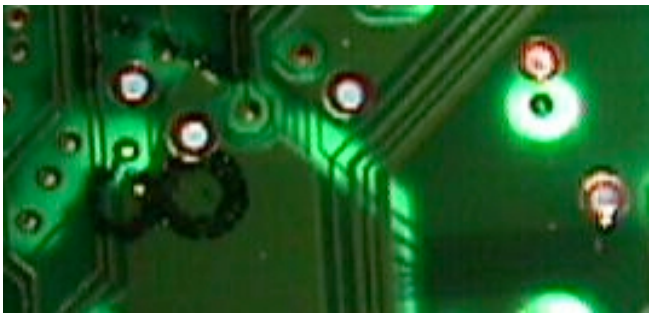

Figure 10. Example of Paths Crossing Break in Ground Plane

Figure 11. Example of Paths Crossing Break in Ground Plane

System Examples and Experiences

Overview

Most companies have some experience in solving system level electrostatic discharge (ESD) problems. This is true especially since ESD is one of the mandatory immunity tests for meeting European requirements to obtain the CE mark. Many of these companies soon realized that front-end device protection or filtering, use of a metallic, well-bonded chassis, or a completely all plastic (insulating)

housing typically will all combine to prevent or solve a majority of these ESD failures.

However, not all ESD potential problems are as obvious as others. Several case histories will be reviewed that point out some of these "less obvious" instances. This review will also serve as a reminder to reinforce some of the more typical ESD solutions as well.[2]

The variety of equipment that information in this paper is derived from ranges from an industrial battery charger, to an external hard drive, to an antenna pattern measuring system, and a medical I/V monitoring device.

Background

The voltage required to break-over through air depends upon several factors, one of which is the shape of the electrode. The worst case situation is for sharp pointed electrodes where the break-over voltage in air is typically less than 1 kV/mm and changes significantly with altitude above sea level. This says that in order to prevent "arcing" through air, we need to keep a physical spacing of at least 8 mm for an 8kV level. This is based upon the most used level 3 criteria of IEC/EN 61000-4-2 of 8 kV for air discharge.

Plastic materials have a dielectric constant that is 2-3 times that of air. The breakdown voltage is usually significantly greater or the minimum separation distance (i.e. thickness) to protect against 8 kV is significantly less than in air. If the dielectric material does not meet its minimum thickness, then a dielectric breakdown could occur through the material. This thickness number can be a strong function of whether the plastic material contains air holes or voids in it.

Dirt, chemicals, dust, and contaminates can draw moisture from the air and form a "conductive" path to a ground point on an insulative surface. The "tracks" flow along the surface of the material looking for a ground discharge point. These tracks can be as long as 50 mm. This author has seen tracks as long as 15 cm in length. This can even happen on a painted surface as the discharge looks for pinholes in the paint. This phenomenon is a particular problem with LCD's, keyboards, and membrane panels. All internal traces should therefore be at least 8 mm removed from any edge.

Case Histories

Several case histories are now presented that illustrate typical ESD situations and some "not so obvious" situations. Most solutions to ESD problems involve good grounding of all exposed metal pieces and or use of plastic materials to avoid ESD occurring in the first place. As we will see the "not-so-obvious" cases usually involve either air/dielectric break-over or "creepage".

LED Body

With more and more enclosures being fabricated from plastic, LED's "sticking out" from the front panel are sometimes forgotten. With a metal front panel, the ESD would arc to the metal panel rather than to the LED causing very little problems. However, with a plastic front panel that metal front panel discharge path is no longer available.

So now, two things can occur (refer to Figure 12). One is that the discharge can actually go right through the plastic lens of the LED directly to the diode chip and leads to the circuit board. The second is that the arc will directly attached itself to the leads of the LED depending upon how far the LED protrudes out the front hole.

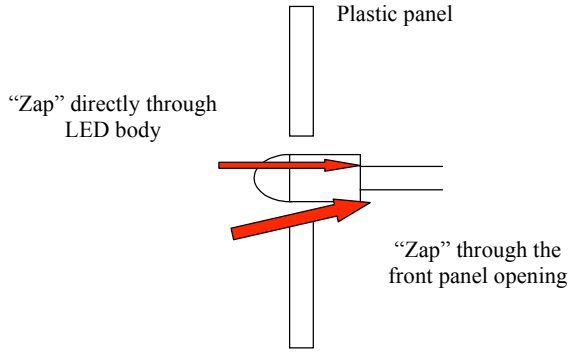

Figure 12. ESD Paths on an LED

So, you should verify that the protrusion of the LED is such that the distance from the front hole opening to the LED leads is at least a minimum of 8 mm if your maximum test level is 8 kV. Remember that the break-over value for air is about 1 kV/mm. Finally, verify what the dielectric strength is for the plastic lens or cover. There are companies that manufacture lens covers that can protect the LED from both potential problem areas.

Small Settable Switches, etc.

The same phenomenon can occur with SCSI settable switches in that arcing could go right through air to the internal conductors of the switch to the circuit board. Again, remember that the air breakdown

voltage value is 1 kV/mm. A small plastic cover of sufficient dielectric strength will usually solve this problem.

So, this situation can apply to any small component that is fabricated out of plastic, but contains metal parts. Any component like this can be a potential victim of this situation (i.e. volume or intensity potentiometers, etc.). Once the arc has occurred, it usually will end up on a lead and any attached PCB where it can create an upset or worst-case, damage a component.

Openings Surrounding Plastic Bezels

The air breakdown problem can also occur on products with an all-plastic front bezel. If there exists a metal insert or backplate behind the plastic bezel, then arcing can occur to the metal by finding air gaps seams (both intentional and unintentional) or voids. In some instances, the discharge "jumped" from the metal insert or backplate and to a PCB located behind this front panel. See Figure 13.

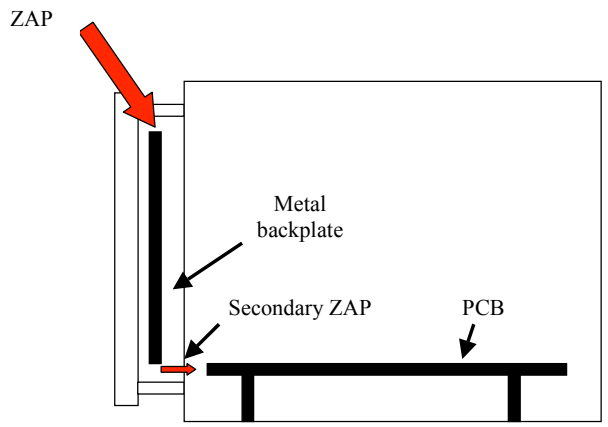

Figure 13. Secondary Arcing

In this case, a conductive coating sprayed directly to the backside of the plastic bezel solved this particular problem. The discharge followed the conductive paint to chassis and the extra separation gained by not having a separate metal plate in between kept the discharge from attaching itself to the PCB.

Isolated Metal Pieces

As discussed in the above section, if a discharge occurs to small isolated metal brackets or panels, these pieces will "charge up" and can cause a re-discharge or secondary arc to some other nearby grounding path such as a nearby PCB. Another concern is that if the isolated metal piece stays charged and it encounters a discharge of the opposite polarity, the effect is a discharge of twice the amplitude !

Screws fall under this category of isolated pieces of metal and can re-radiate the ESD energy as electromagnetic fields that can couple to internal circuits or wires. In other words, they can act as antennas. A good design would make sure that no screws are left protruding on the inside of the chassis to radiate the ESD noise.

If connectors are the PC-mountable types, the connector shells must be well grounded to the chassis or else discharge currents could find a path through the PCB by attaching to nearby traces. An inadequately grounded connector shell will also cause very high-localized field intensities that can easily couple noise into the connector wires.

Single Point Grounding

Electrostatic discharges contain reasonably high frequency content. The frequency components can reach well beyond several hundreds of Megahertz. Therefore, the physical dimensions of most devices are significant fractions of the wavelength of the higher frequency components. As an example, the wavelength of 300 MHz is about one meter. A significant fraction of a wavelength is from 1/8 of wavelength to 1/4 of a wavelength. This yields a dimension of about 10-25 cm. What this implies is that if a PCB is grounded in only one point, it is susceptible to common mode potential between the PCB and the chassis.

To solve this problem, the PCB has to be multi-point grounded to "tie" the PCB better, common mode wise to chassis. This will prevent currents from flowing across the PCB. If multiple, direct connections to chassis are not allowed, then ground the PCB through multiple good high frequency capacitors.

Physical Separation

I don't think we have to say much more here since we have already discussed the air breakdown criteria. Just make sure that the dielectric strength or wall thickness and separation distance to the nearest conductive part can withstand your voltage requirement. Look at Figure 14 for some examples.

"Non-Conductive" Items

As final example of "not-so-obvious" cases, consider that air discharges have occurred on non-conductive surgical tubing of an I/V Drip & Temperature Monitor. No liquid was flowing at the time.

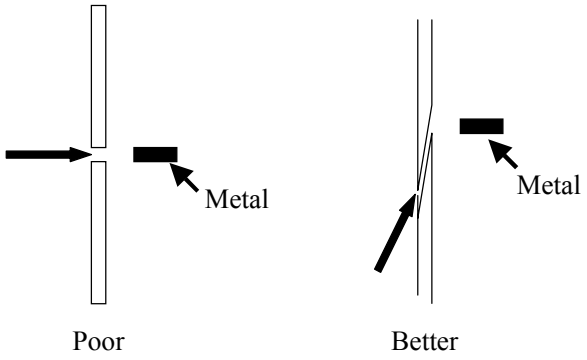

Figure 14. Increasing Physical Spacing

In the first part of this paper, we discussed how ESD can "creep" along an insulative surface. Dust, dirt, oils, etc. can draw moisture from the air and provide conductive paths. You can see this for yourself by taking a piece of plastic and running the ESD gun over the surface of the plastic. You will see trails of energy flowing over the surface much like a Kerlian photograph. This works better in a darkened room. At greatest risk for this phenomenon are membrane switches. There can still be dielectric breakdown possibilities through the insulative material to any metallic switch parts, but it is easy to ignore this "creepage" problem. The ESD can flow along the surface for several inches in order to find a ground discharge path. This can easily be a trace too near the edge of the membrane switch layer construction.

Further Work

One potential area of additional work suggested by results in this paper relates to the effect of a path that crosses through two ground/power planes. The closer the planes and the better the bypassing or connection between the two, the lower the interplane impedance will be. The lower this impedance, the less will be the effect noted in Figure 5. This experiment should be performed on a typical 4 layer PWB to see the effect on ESD immunity of a signal crossing from the top layer to the bottom layer. This is a very common layout practice with the potential result of compromised ESD immunity.

Conclusions and Summary

Data and examples have been presented that show how important good design practices are to the ESD immunity of an electronic system. Often these design practices are very inexpensive or even free if included early in system design. However, added after the design is complete or in production, these techniques can add significant cost and schedule delays to a system.

The authors hope that this paper raises awareness of these issues in the design community.

References

[1] *High Frequency Measurements and Noise in Electronic Circuits*, Seminar by Douglas C. Smith, http://www.dsmith.org.

[2] *Electrostatic Discharge: Understand, Simulate, and Fix ESD Problems*, 2nd Edition. 1992, Michael Mardiguian, Interference Control Technology, Inc. Gainsville, VA, ISBN: 0-932263-27-5